IN THE SPECIFICATION

Please amend paragraph [0025] on p. 14 of the Specification as follows:

-- For example, two independent compare instructions 031, 032, shown above in Table 3, must be executed sequentially because the compare instruction 031 not only writes to predicates p1 and p2 but all 64 predicates of the predicate register file, including the predicates p3 and p4. Thus, the instruction 032, which reads and modifies predicates p3 and p4, must wait for the completion of the instruction 031. Accordingly, to process more than one compare per clock cycle, a fusing mechanism may be employed. This fusing mechanism is further described in a related U.S. Patent Application Serial No. ~~_____,~~ 10/335,201, filed by inventors Grochowski *et al.*, ~~Intel Matter Number P12585,~~ entitled "Fuser renamer apparatus, systems, and method~~Method and Apparatus for Fusing Multiple instructions/ Microops into One~~."--